Design of a digital four-terminal-pair impedance bridge

Waldemar G. Kürten Ihlenfeld, Renata T. de Barros e Vasconcellos

Instituto Nacional de Metrologia, Qualidade e Tecnologia - Inmetro

E-mail: wgkihlenfeld@gmail.com

Abstract: The paper describes the design of a four-terminal-pair impedance bridge developed at INMETRO. Originally devised to work as a quadrature bridge for deriving the unit of capacitance (Farad) from a resistance (Ohm) or vice-versa, it allows the comparison of impedances in general with outstanding accuracy and measurement uncertainties bearing some 10^{-06} Ω/Ω.

Keywords: Impedance, digital signal processing, measurement standards, dissipation factor, time-constant.

1. INTRODUCTION

In the last decades, metrologists could witness the immense progresses done in the development of electronic signal -acquisition and -synthesis devices known as analog-to-digital (ADCs) and digital-to-analog converters (DACs) allied with advances in digital signal processing techniques. The superb performance of modern devices is the result of intense and expensive worldwide research efforts in many research institutes and industries, impulsed by prodigious technological advances in the semiconductor industry. Meanwhile, these techniques inspired further developments in Metrology as well. The possibility of comfortably digitizing alternating (ac) signals with high resolution and accuracy is reality today and something for that metrologists were long craving. Undoubtedly, digital signal processing techniques will somewhen dominate Metrology, also the field of ac-impedance measurement, where cumbersome, difficult-to-use, and time-consuming manually operated analog-coaxial-ac-bridges became essential as primary standards. Albeit the astonishing accomplishments done in electronics and specifically in the field of ADCs and DACs, it will indeed take some time for the digital techniques to conquer part of the field dominated by their analog counterparts, which are still able to guarantee high-grade measurements with nearly unbeatable uncertainties of only some parts of 10^{-09} Ω/Ω. Digital bridges are however on the march and overtaking niches in scientific and industrial metrology.

We describe next, development efforts done at INMETRO in designing a digital sampling impedance bridge. It employs a new and patent pending synchronization algorithm that allows digital phase-synchronization of digitally synthesized signals balancing the bridge with nano-radian resolution to be attained.

2. HARDWARE DESCRIPTION

The system evolved from a first approach as described in [1,2]. Latest developments lead to further improvements in hardware (and software),

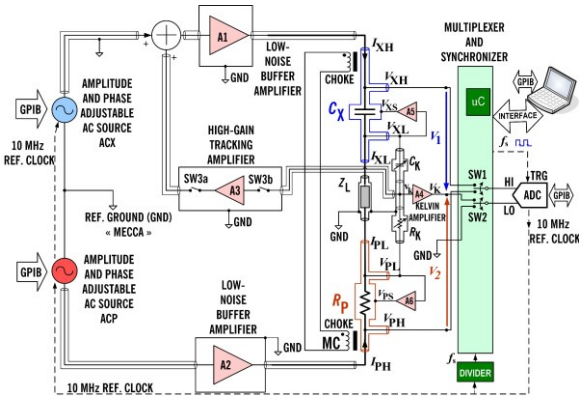

Figure 1. Complete diagram of the digital ac impedance bridge that works as a voltage comparator. It is composed of a main arm with impedances C_X and R_P, electrostatically shielded amplifiers, a C_KR_K Kelvin arm, and a multiplexer with a synchronizer for coherent sampling of voltages with the internal 10 MHz of a 28-bit ADC. A personal computer (PC) controls the whole system (see text for further details).

which culminated with the complete diagram as shown in figure 1.

The development started with the design of low-ripple direct current (dc) voltage sources that supply its amplifiers. Ideally, each amplifier should possess its own dc supply to avoid undesired coupling and crosstalk during operation; however; only two dc power sources of higher capacity were used to supply each of the amplifiers that deliver current to the bridge (A1 and A2) to a maximum of 250 mA and 10 V amplitude. A third dc source was reserved to supply the remaining amplifiers, which work only with signals of small magnitudes and low power (A3 to A6). The use of toroidal power transformers with an electrostatic shield (tied to a common power-network ground) between the primary and secondary windings is mandatory.

Special attention was devoted to the analog grounding, which is a large area of a plated circuit board (PCB) of very low inductance that accommodates the analog amplifiers and the relays of the multiplexer. Amplifiers´ supply terminals are decoupled with bypass capacitors (of foil and ceramic type capacitances). Amplifiers´ reference- grounds are tied to a single common ground point called “Mecca”, which is a judiciously chosen single zero reference point of the large low-inductance ground area of the PCB, so that voltage drops due to ground loop currents do not significantly impair measurements. Electrostatic shielding and the use of coaxial cables preclude other deleterious coupling effects to become noticeable, such as those caused by unavoidable stray capacitances among amplifiers and their wirings up to the main arm set up by the four-terminal-pair coaxial standards C_X and R_P. The definition of a four-terminal pair impedance standard requires, as the name suggests, four coaxial inputs for C_X and R_P as follows. 1) Current “high terminals” (I_{XH} and I_{PH}) with nearly equal input currents by proper adjusting the ac sources ACX and ACP, aided by the use of a choke that uses a high permeability magnetic core MC as shown in figure 1. 2) Voltage “high terminals” V_{XH} and V_{PH} from which negligible current shall be drawn out. 3) Voltage “low terminals” V_{XL} and V_{PL} which must display – by definition – zero voltage with respect to the voltages of the metal enclosures of the standards V_{XS} and V_{PS} respectively, i.e., $V_{XS} = V_{XL}$ and $V_{PS} = V_{PL}$. The unity-gain field effect transistor (FET) buffer amplifiers A4 and A5 ensure that these conditions hold. 4) Current “low terminals” I_{XL} and I_{PL} from which currents are driven out of the elements satisfying the equality $I_{XL} = I_{PL}$. Ideally, the connection of both terminals I_{XL} and I_{PL} should become a single point. This is though not attainable in the practice, and a coaxial cable of some centimeters in length (and of line impedance Z_L) provides the electrical connection of both standards. In equilibrium, V_{XH} is exactly 90° out of phase with respect to V_{PH}, so that the currents through I_{XL} and I_{PL} nearly annihilate each other. Although Z_L is small but not negligible, the voltages V_{XL} and V_{PL} do not vanish either. Their amplitudes amount to some tens to hundreds of microvolts, depending on the quality of the adjustment of ACX and ACP. A divider built by

the Kelvin arm C_K and R_K compensates for the voltage difference between V_{XL} and V_{PL} and for the undesired effects of Z_L. These effects are minimized when the time constant $R_K C_K$ is equal to that of $R_P C_X$, resulting in a feeble voltage signal v_K at the junction joining R_K and C_K. The negligible impedance loading of the Kelvin arm with C_K in series with R_K and in parallel with Z_L has only negligible second-order effects on the voltages V_{XL} and V_{PL}, since their magnitudes are feeble and Z_L is small. However, any loading effect due to the multiplexer and the ADC´s finite input impedance at the v_K-point would wreak havoc compensation measures for Z_L. For this reason, the FET unity-gain buffer amplifier A4 (called the Kelvin amplifier) is used for impedance matching keeping $v_K = V_K$ (at A4´s output). Nearly perfect compensation due to Z_L is thus attained by sampling the differential voltages $V_1 = V_{XH} - V_K$ and $V_2 = V_{PH} - V_K$.

The synchronizer is controlled by a micro-controller interfaced to a PC and controls the analog parts of the bridge via opto-couplers and the multiplexer, which allows the direct and differential sampling of voltages of the bridge. Direct sampling is accomplished with the switch SW1 multiplexing the ADC's HI terminal synchronously between V_{XH} and V_{PH} over M integer positive periods and triggering the ADC to acquire N (integer) equally time-spaced samples per period with SW2 tying the ADC's LO terminal to the Mecca ground. The differential sampling of voltages V_1 and V_2 is done by tying the ADC´s LO to V_K via SW2 with SW1 multiplexing the ADC´s HI between V_{XH} and V_{PH} as before. The direct and differential sampling serves different purposes. The direct sampling is used to phase-synchronize the ac sources ACX and ACP by software to balance the bridge ($V_K \approx 0$). The differential sampling is used to obtain equally time-spaced samples of V_1 and V_2, which are fast Fourier-transformed (FFTed) and used to calculate a complex ratio $(A + jB)$ = {FFT of the data vector of V_1 samples}/{FFT of the data vector of V_2 samples} at the angular frequency $\omega = 2\pi f$, and fundamental frequency f. This ratio is essential for determining the parameters of the unknown element C_X including its dielectric tangent delta "tanδ" or dissipation factor D, once R_P and its time-constant τ are known according to [1]:

$$C_X = \frac{1}{\omega \cdot R_P \cdot (B + j\omega\tau A)} \qquad (1)$$

$$D = \tan\delta = \frac{B\omega\tau - A}{B + \omega\tau A} \qquad (2)$$

The bridge imposes stringent requirements on amplitude, phase stability over time and harmonic content of the ac sources ACX and ACP. Although ordinary workbench synthesizers are able to maintain frequency and phase stability by frequency locking them to a common reference 10 MHz clock (extracted from the ADC), the same cannot be assured about their amplitude stability, which may vary by as much as 0.1% in a short interval between measurements. To partially counteract voltage variations of either ACX or ACP, a FET tracking amplifier A3 can be engaged via SW3 (controlled by the PC via synchronizer) to feed-back such variations by sensing the corresponding v_K fluctuations, highly amplifying and adding them to the input of A1, closing a negative feedback loop. As a result, the magnitude of v_K (and thus of V_K) is sensibly reduced and any fluctuation either of ACX or ACP become highly correlated, what reduces their effects on ratio measurements. This tracking effect allows high accuracy and precision to be attained even with ubiquitous workbench synthesizers of poor accuracy and amplitude stability. This is an excellent prospective benefit of this approach for secondary calibration laboratories.

The use of amplifiers A3 to A6 emphasizes novelty and improved performance not attained by other developments [3,4] as demonstrated by investigations on the metrological validation [5] of

the bridge in figure 1. In this case, we were lead to conclude after solid investigations and reasoning that the use of special high grade digital signal synthesizers as ac sources of exceptional stability in amplitude of some 10^{-6} parts, high sine purity and tight phase locking capability, allied with low noise content will enable measurement accuracy and repeatability below some parts of 10^{-07}. This work is still in progress.

3. DESCRIPTION OF THE SOFTWARE

The control software in C++ provides setup adjustments, data –acquisition, -processing, and -protocolling. Nominal numerical values of C_X and R_P are inputs for a coarse adjustment of the ac sources ACX and ACP by calculation. A finer adjustment by software uses a searching algorithm known as Downhill simplex [6]. In case the user wants to use the tracking amplifier, a coarse adjustment in amplitude suffices without the Downhill simplex method. The phase between the signals of ACX and ACP sources must however be adjusted accurately to balance the bridge. This is done by a patent pending algorithm that allows phase adjustments up to some nano-radian to be attained, depending on the noise present in the sampled data. This process relies on the tight frequency synchronization of the ac sources and the synchronizer that enables coherent sampling at a rate f_s with the ADC reference clock via a divider (see figure 1). By direct sampling the two arm voltages V_{XH} and V_{PH}, a phase deviation is computed from their FFT-data and a fractional frequency correction of high resolution is applied to one of the sources by programming it with a new frequency over a finite time span. A very precise phase shift is thus produced. This builds up a feedback loop, which is best controlled by digital regulators. A detailed treatment of this algorithm is described in [7] for DACs and in [8] for ADCs (when a reference or master clock is not available).

4. CONCLUSIONS AND OUTLOOK

The metrological validation [5] of our bridge demonstrates its high-grade performance yielding uncertainties of only some 10^{-6} parts. Work is in progress to hone its capabilities towards even lower uncertainties of 10^{-7} to 10^{-8} parts.

5. REFERENCES

[1] Ramm G and Moser H. From the classical ac resistor to the capacitor – dissipation factor measurements on the basis of time constants. *Proc. CPEM 2000*. 2000 Jun; 133-134.

[2] Kürten Ihlenfeld W G and Vasconcellos R T B. A digital quadrature bridge for impedance measurements. *Proc. CPEM 2014*. 2014 Aug; 106-107.

[3] Overney F and Jeanneret B. RLC Bridge Based on an Automated Synchronous Sampling System. *IEEE Trans. Instrum. Meas.* 2007 Jul; 60(7): 2393-2398.

[4] Callegaro L and D'Elia V et al. Experiences with a two-terminal-pair digital impedance bridge. *IEEE Trans. Instrum. Meas*. 2015 Jul; 64(6): 1460-1465.

[5] Vasconcellos R T B and Kürten Ihlenfeld W G. Ac resistance measurements using digital sampling techniques. To appear in *Proc. XI Semetro*. 2015 Nov;

[6] Press W H, Vetterling W T, Teukolsky S A and Flannery B P. Numerical Recipes in C++ - The Art of Scientific Computing. 2nd ed. New York: Cambridge University Press; p. 398-448.

[7] Kürten Ihlenfeld W G and Landim R P. An automated Josephson based ac-voltage calibration system. *IEEE Trans. Instrum. Meas.* 2015 Jul; 64(6): 1779 – 1784.

[8] Kürten Ihlenfeld W G and Seckelmann M. Simple algorithm for sampling synchronization of ADCs. *IEEE Trans. Instrum. Meas.* 2009 Apr; 58 (4): 781–785.